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Remarks:

Reconsideration of the application is respectfully requested.

Claims 1 - 13 are presently pending in the application. As it is believed that the claims were patentable over the cited art in their original form, the claims have not been amended to overcome the references.

In item 3 of the above-identified Office Action, claims 1 - 5, 7 - 10, 12 and 13 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,477,674 to Bates et al. ("**BATES**"). In item 4 of the Office Action, claim 6 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **BATES** in view of U. S. Patent No. 6,704,897 to Takagi ("**TAKAGI**"). In item 5 of the Office Action, claim 11 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **BATES** in view of U. S. Patent No. 5,751,151 to Levy et al ("**LEVY**").

Applicant respectfully traverses the above rejections.

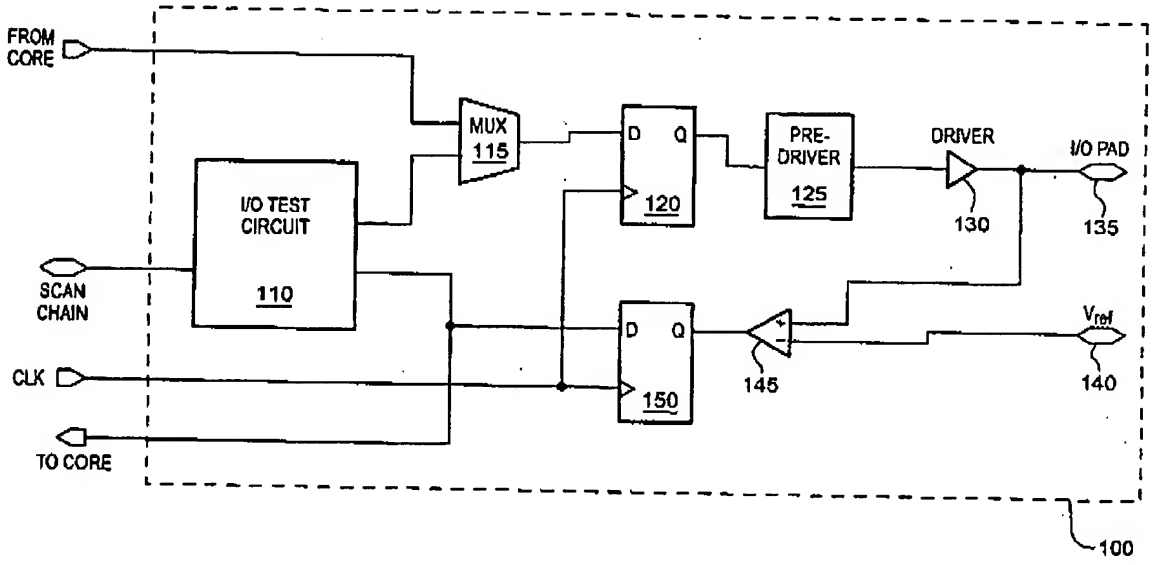
More particularly, claim 1 recites a semiconductor module with a configuration for the self-test of a plurality of bidirectionally operating interface circuits, including among other limitations:

> a first circuit connected to said first group and **serving to generate test signals** to be multiplexed in **and output via said interface circuits of said first group;**
>
> a second circuit connected to said second group **for receiving and processing test signals received via said interface circuits of said second group** [emphasis added by Applicant]

Applicant's claim 7 includes all of the limitations of Applicant's claim 1, by reference to that claim, among other limitations.

As such, all of Applicants' claims require, among other limitations, **that test signals in the first group of bidirectionally operating interface circuits be outputted to, and received by, the second group of interface circuits.** Among other limitations of Applicant's claims, **BATES** neither teaches, nor suggests, among other limitations of Applicant's claims, a first group of bidirectionally operating interface circuits outputting test signals to a second group of bidirectionally operating interface circuits, since, in **BATES, each interface circuit is self-testing.** Thus, in **BATES**, each I/O buffer 100 of **BATES, being self-testing, does not, and cannot, transmit test signals to, or be assigned to communicate test signals to, any other I/O buffer 100 of BATES.**

As discussed in Applicant's reply of December 6, 2005, **BATES** discloses the input/output buffers 100 each include **a test circuit 110** for performing a self-test of **the respective** input/output buffer. This test is referred to as the "I/O loopback test" in **BATES**, col. 1, line 33, col. 2, line 47, column 3, lines 34 and 48 and column 6, line 25. Fig. 1 of **BATES** is reproduced herebelow, for convenience.



Referring now to Fig. 1 of **BATES**, a respective buffer 100 is tested during the I/O loopback self-test to determine whether the respective buffer is defective. As such, the loopback self-test of **BATES** performs a test **within, and only within, the respective buffer** 100's electrical path, i.e., including elements 115, 120, 125, 130, 145, 150, 110 **to test if the respective buffer is operating properly.** In particular, in the test mode of **BATES no test signals leave a respective**

buffer 100 under test, for example, via the input/output pad 135 (Fig. 1 of **BATES**), **since only the electronic components internal to each respective buffer 100 are tested.**

Further, Fig. 2 of **BATES** illustrates a detailed view of the I/O test circuit 110 which serves to generate the test pattern signals. Fig. 2 of **BATES** is additionally being reproduced herebelow, for convenience.

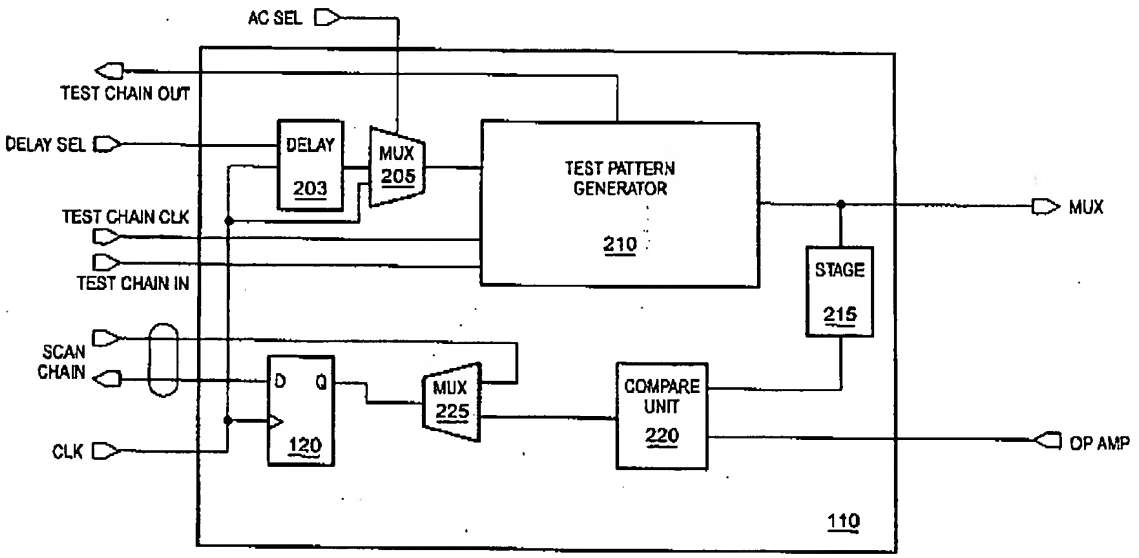


FIG. 2

BATES' test circuit 110 includes a test pattern generator 210, an output line connected to MUX 115 of the buffer 100 (compare Figs. 1 and 2 of **BATES**) and an input line for receiving input signals incoming from amplifier 145 (compare Figs. 1 and 2 of

BATES; and col. 3, lines 62 - 64 of **BATES**). Further, the test circuit 110 illustrated in Fig. 2 OF **BATES** (and provided **in each** input/output buffer 100, as illustrated in Fig. 1 of **BATES**) **includes a stage 215**. Col. 3 of **BATES**, lines 60 - 64, states:

> According to one embodiment, **stage unit 215 provides a one cycle delay for the test pattern signals before they are transmitted to compare unit 220** be compared with test signals received from amp 145.

As such, the stage unit 215 of **BATES** serves to **directly connect** the generated test pattern signal to the compare unit 220 of **BATES**. See **BATES**, Fig. 2. In this way, **BATES** provides a duplicated test pattern signal for comparison with the signal received from amplifier 145. See **BATES**, col. 5, lines 65 - 67.

In reviewing Fig. 1 and 2 of **BATES in context with one another**, it is apparent that **each buffer 100 includes a test circuit 110 internally generating a test signal**, which, in the form of a first **duplicate** signal, is passed across elements 115, 120, 125, 130, 145, 150 **within the respective buffer 100**, before again arriving in the test circuit 110 for **internal** comparison in the compare unit 220. The second duplicate signal is sent directly within the test circuit 110 to the stage 215, and from the stage 215 to the compare unit 220. Note that **each** buffer 100 shown in Figs. 1 and 5 of **BATES**,

must include its own, respective test circuit 110, which **only** serves to **internally** test the **respective** individual buffer 100.

As such, in **BATES, during the self-test of each respective buffer, no test signals from the buffer 100 under test are forwarded to any other buffer 100 of BATES**. In particular, during the self-test mode for a particular buffer in **BATES, no test signal leaves the respective buffer** 100 via the input/output pad 135 **or being sent to an input/output pad 135 of a second respective input/output buffer**.

Thus, the **BATES** reference fails to teach or suggest, among other limitations of Applicant's claims, the transfer of **test signals** from a first interface circuit to a second interface circuit. Rather, in alleging the obviousness of this limitation of Applicant's claims over **BATES**, pages 4 - 5 of the Office Action stated, in part:

> Bates does not explicitly teach "first and second equally sized groups of interface circuits, wherein each interface circuit of said first group is assigned exactly one interface circuit of said second group" and "**a first circuit connected to said first group and serving to generate test signals to be multiplexed in and output via said interface circuits of said first group; a second circuit connected to said second group for receiving and processing test signals received via said interface circuits of said second group**". However, Bates does teach I/O buffers 100(1)-100(n) make up a data block of I/O circuitry for transmitting to and receiving data from other IC 100 devices (first

> and second equally sized groups of interface circuits). **(Col. 4, ll. 28-32)**. In Figure 5, which is a block diagram of one embodiment of an integrated circuit (IC) 500 that includes input/output (I/O) buffers 100(1)-100(n). I/O buffers 100(1)-100(n) make up a data block of I/O circuitry for transmitting to and receiving data from other IC 100 devices. Bates continues to teach that a data block includes sixteen (16) I/O buffers 100. However, in other embodiments, a data block may include other multiples (e.g., 2, 4, 8, 12, 18, 32, 40 64, etc.) of I/O buffers 100. (Col. 4, ll. 28-37)
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made that the "other IC 100 devices" Bates is referring to, as interpreted by the Examiner, is a duplication of IC 500 that includes other groups of input/output (I/O) buffers 100(1)-100(n), which qualifies the "other IC 100 devices" as the second group. The artisan would be motivated to do so because the I/O buffers 100 (i.e. as well as other IC 100 devices) are groups that are duplicated and therefore, comprises the same number of input/output buffers as the first group. [emphasis added by Applicant]

Applicant respectfully disagrees that the claimed subject matter is obvious over **BATES**. For example, **taking, arguendo, everything said on pages 4 - 5 of the Office Action as correct** (although, Applicant does not agree that the statements are correct and reserves the right to contest it) **the Office Action has still failed to teach, suggest or motivate one skilled in the art to transmit test signals from one of the interface circuits of the first group to one of the interface circuits of the second group**, as required by Applicant's claims. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention **where there is some teaching, suggestion or**

motivation to do so found either **in the references** themselves or **in the knowledge** generally available to one of ordinary skill in the art. Such a teaching, suggestion or motivation is not found in the present case.

For example, the Office Action cites to col. 4 of **BATES**, lines 28 - 32, as allegedly providing the motivation to amend **BATES** to transmit **test signals** from one IC 100 to another IC 100. Applicant respectfully disagrees. More particularly, col. 4 of **BATES**, lines 28 - 32, state

> FIG. 5 is a block diagram of one embodiment of an integrated circuit (IC) 500. IC 500 includes input/output (I/O) buffers 100(1)-100(n). **I/O buffers 100(1)-100(n) make up a data block of I/O circuitry for transmitting to and receiving data from other IC 100 devices.** [emphasis added by Applicant]

However, the above-cited portion of **BATES** only refers to the **normal mode** of operation of the **BATES** devices, and **not** to the **test mode**. More particularly, **BATES** discloses, in col 2 of **BATES**, lines 60 - 63, that an I/O buffer 100 communicates with (or is assigned to) another I/O buffer 100 only **in the 'normal mode'** of operation. See, also, col. 2 of **BATES**, line 48. This transfer does **not** occur in **BATES** when the devices are in the **'self-test mode' of BATES**.

Similarly, col. 4 of **BATES**, lines 50 - 54 also clearly states that the **normal mode** of **BATES** (mentioned in line 50), **rather**

than the test mode of **BATES, is the mode in which a communication between the I/O buffers occurs.**

Since **BATES** only discloses that the ICs 100 communicate with each other **in the normal mode**, while specifically teaching that each I/O buffer 100(1) through 100(n) of **BATES only conducts internal testing during the test mode** (i.e., each buffer only tests itself), a person of ordinary skill in the art, reading **BATES** would **not** receive any teaching, suggestion or motivation for the ICs 100 to communicate with each other **during the self-test mode** of **BATES**. It does not make sense to transmit test signals between two groups of I/O buffers, during the **self-testing** of the I/O buffers, as disclosed by Bates. In **BATES**, test signals are **not** generated by a first group of I/O buffers **for testing a second group** of I/O buffers. Instead, in **BATES**, all test signals are generated, transmitted and compared within (i.e., internally to) each respective I/O buffer, while testing **itself**. Accordingly, Applicant believes that the **BATES** reference would **not** provide a teaching, suggestion or motivation, contrary to the statement made on page 4 of the Office Action, to modify **BATES** in the manner suggested in the Office Action. In fact, **BATES** would teach away from Applicant's claimed invention, by clearly requiring testing to occur **only** within each I/O buffer

100(1) - 100(n) (i.e., thus making use of the test signals of one I/O buffer **only** internally to **that** I/O buffer).

In **BATES**, since each I/O buffer 100 is self-testing, it generates its own test signals, forwards the test signal throughout **its own** I/O buffer components, and finally **internally** compares the forwarded test signal with the initially generated test signal. **BATES** neither teaches, nor suggests, nor requires any second I/O buffer to be involved in in the self-test performed by any other I/o buffer, since the route of propagating the test signals (along the components 115, 120, 125, 130. 145 and 150 of Fig. 1 of Bates, as discussed above) completely extends **within** the respective I/O buffer, and does not include any communication with any second buffer I/O. As disclosed in **BATES**, each I/O buffer 100(1) - 100(n) of Fig. 5 of **BATES**, performs the self-test in the manner described in connection with the I/O buffer 100 of Fig. 1 of **BATES** (i.e., only using those components arranged **within** the I/O buffer under test). Accordingly, each I/O buffer 100(1) - 100(n) of Fig. 5 of **BATES** is testing **only itself**, in order to perform a complete I/O-buffer-internal self-test. As such, for this technical reason, **BATES** does **not** teach, suggest or require, any **assignment, during testing**, of a first I/O buffer to any second I/O buffer, as required by Applicant's claims. As stated above, **BATES** only discloses communication

between the I/O buffers 100(1) - 100(n) **when the device is operating in the normal mode** (i.e., not the test mode), and thus, **BATES** does **not** teach, suggest or motivate the transmission of **test signals** from one I/O buffer to another I/O buffer.

Further, in contrast to the statement made in the Office Action, Applicant believes that col. 4 of **BATES**, lines 28 - 32, does not even teach or suggest that the I/O buffers 100(1) to 100(n) of Fig. 5 of **BATES** could be assigned to a second group of buffers 100(1) to 100(n) of the **same**, semiconductor module (or integrated circuit) 500. More particularly, Applicant's claim 1 requires, among other things, that the **semiconductor module include two equally sized groups of interface circuits**. However, any I/O buffer of another semiconductor module does not belong to the illustrated semiconductor module 500. Thus, the semiconductor module of **BATES** fails to teach or suggest, among other limitations of Applicant's claims, **more than one group of I/O buffers provided on the semiconductor module 500**. Accordingly, it would not be obvious, in view of the failures of the teachings of **BATES**, to provide a 'second, equally sized' group of I/O buffers **on the same semiconductor module**.

The disclosure in col. 4 of **BATES**, lines 28 - 32 (cited in the

Office Action as allegedly providing the motivation to modify **BATES**) must be read in its particular context and in view of the whole document. In context, the **BATES** reference discloses: (1) in the testing mode, **self**-testing each I/O buffer by itself, without any assignment to any other I/O buffer; and (2) in normal mode, possibly communicating information from one I/O buffer to another I/O buffer of **other, distinct semiconductor modules only** (i.e., **BATES** does not teach or suggest providing any second group of I/O buffers on the same semiconductor module 500, contrary to Applicant's claimed invention).

In fact, it is stated on page 4 of the Office Action, that the Examiner interprets the "other IC 100 devices" of **BATES** to be **a 'duplication' of integrated circuit 500** including 'other groups' of I/O buffers. However, each duplicated IC 500 would include **only one**, single group of I/O buffers, just like the integrated circuit 500. Thus, this duplicated integrated circuit 500 would not form any part of the original integrated circuit 500. As stated above, Applicant's claims recite, among other things, **a semiconductor module** including **two** equally sized groups of I/O buffers assigned to one another and forming part of the same integrated circuit. Such duplication, as "interpreted" by the Examiner, would place the second, equally sized group of I/O buffers **on a different**

semiconductor module, rather than on the **same** semiconductor module, thus neither teaching, nor suggesting, Applicant's claimed invention.

In summary, among other things, **BATES** fails to teach, suggest or motivate a person of skill in this art to communicate between I/O buffers at times other than the normal mode of operation. Thus, the I/O buffers of **BATES** do **not** communicate with each other in test mode. Further, the person of skill in the art would be taught away from modifying **BATES** to communicate **test signals** between I/O buffers, because **BATES** discloses that **each** I/O buffer internally tests, itself (i.e., performing the self-test exclusively by using components arranged within the particular I/O buffer under test). As such, the I/O test circuit 110 of Fig. 2 of **BATES** (also forming part of the self testing I/O buffer 100 of Fig. 1 of **BATES**) only serves for generating the test signal and comparing the original test signal with the test signal received after loopwise transmission thereof along the components 115,120,125.130,145,150, **internal to** the I/O buffer 100 under test. Note that the multiplexer 115 of Fig. 1 of **BATES** only serves to switch the I/O buffer 100 between normal mode and test mode. See, for example, col. 2 of **BATES**, lines 45 - 48.

In view of the foregoing, it can be seen that Applicant's claimed invention is not obvious over **BATES**. The **TAKAGI** and **LEVY** references, cited in the Office Action in combination with **BATES** against certain of Applicant's dependent claims, do not cure the above-discussed deficiencies of the **BATES** reference. As such, Applicant's claims are believed to be patentable over **BATES**, **TAKAGI** and **LEVY**, whether taken alone, or in combination.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claim 1 and 7. Claims 1 and 7 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 7.

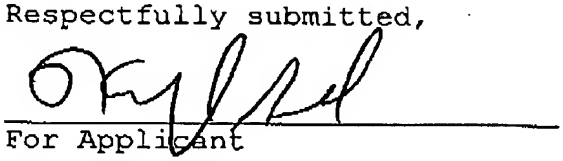
In view of the foregoing, reconsideration and allowance of claims 1 - 13 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



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